WHAT IS CLAIMED:

1. A semiconductor device comprising:

a substrate having a doped semiconductor region, a gate wiring, a lower conductor structure, an insulating layer overlying said lower structure and having at least one through opening extending to said lower conductor structure, and an upper conductor structure connected to said lower conductor structure via said through opening, wherein said upper structure comprises: at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide or a conductive oxide film, and an electroplated or electrolessly plated ~~a~~ metal plating layer disposed on and adhering to said at least one layer.

2. A device as defined in claim 1 wherein said at least one layer consists of a single layer.

3. A device as defined in claim 1 wherein said at least one layer comprises a combination of at least two layers, each said layer being of a respective one of said recited materials.

4. A device as defined in claim 1 wherein said metal plating layer comprises at least one of Cu, Ni, Au, Cr, Co, Rh, Pd and a solder material.

5. A device as defined in claim 4 wherein said metal plating layer is an electrolytically plated ~~onto said at least one~~ layer.

6. A device as defined in claim 4 wherein said metal plating layer is an electrolessly plated ~~onto said at least one~~ layer.

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7. A device as defined in claim 1 wherein said metal plating layer comprises a combination of an electroplated layer and an electrolessly plated layer.

8. A device as defined in claim 1 wherein said metal plating layer comprises at least two alloy plating layers.

9. A device as defined in claim 1 wherein said metal plating layer comprises a superposed combination of a first plating layer composed of a single metal and a second plating layer composed of an alloy.

10. A device as defined in claim 1 wherein said metal plating layer is formed electrolytically by application of one of a direct current, an alternating current, an intermittent current and a periodically reversing current.

11. A device as defined in claim 1 wherein said doped semiconductor region is an impurity doped Si monocrystalline region.

12. A device as defined in claim 1 wherein said metal plating layer is disposed only within said through opening.

13. A device as defined in claim 12 wherein said metal plating layer is an electrolessly deposited layer of Cu, Ni, Au, Cr, Rh, Pd, or soldering material.

14. A device as defined in claim 13 wherein said metal plating layer conductively connects at least one of said gate wiring and said lower conductor structure to said upper conductor structure.

15. A device as defined in claim 12 wherein said metal plating layer a plurality of superposed layers of respectively different materials.

16. A device as defined in claim 12 wherein said metal plating layer is composed of an alloy.

17. A device as defined in claim 1 wherein said gate wiring and said lower conductor structure are composed of a conductive layer of polysilicon, metal silicide, metal polycide, refractory metal, or a metal of the Al series.

18. A device as defined in claim 17 wherein said gate wiring and said lower conductor structure further comprise a metal plating layer deposited on said conductive layer.

19. A device as defined in claim 17 wherein said metal plating layer is formed at said gate wiring and said lower conductor structure.

20. A device as defined in claim 1 wherein said lower structure comprises: at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide or a conductive oxide film, and a metal plating layer disposed on and adhering to said at least one layer.

21. A semiconductor device comprising:

a substrate having a doped semiconductor region, a layered gate member, a lower conductor structure, an insulating layer overlying said lower structure and having at least one through opening extending to said lower conductor structure, and an upper conductor structure connected to said lower conductor

structure via said through opening, wherein said upper structure comprises: ~~a~~ an electroplated or electrolessly plated metal plating layer formed in said through opening; and a conductor structure component formed on said metal plating layer and on said insulating layer.

22. A device as defined in claim 21 wherein said conductor structure component is composed of two-layers, with at least one of the two layers being a further metal plating layer.

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